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| **Lab No** | 02 |
| **Instructor Name** | Dr. Andy Ye |
| **Section No** | 06 |

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| **Name** | **Student ID** | **Signature\*** |
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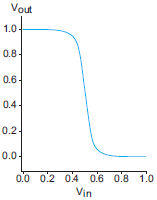
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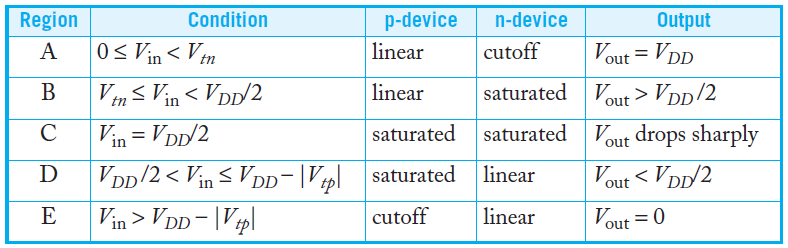
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# **1. Pre-Lab**

## 1.1. Transfer Function of a CMOS Inverter



### *Figure 1: CMOS Inverter DC Characteristic [1]*



### *Table 1: Summary of CMOS Inverter Operation [1]*

The inverter is Figure 1 is an un-skewed inverter with beta ration r=1. The input threshold voltage for the inverter in Figure 1 is VDD/2.

The formula for skewed inverters with varying beta ratios is .

A HI-skew inverter (r>1) has a stronger pMOS transistor. Therefore, if the input is VDD/2, we would expect the output will be greater than VDD/2. Thus, the input threshold for a HI-skew inverter must be higher than that of an unskewed inverter.

A LO-skew inverter (r<1) has a weaker pMOS transistor and thus a lower switching threshold.

A HI-skew inverter shifts the DC Characteristic graph to the right for an un-skewed inverter. Similarly, a LO-skew inverter shifts the DC Characteristic to the left for an un-skewed inverter.

## 1.2 Expression Derivation for an Ideal Static CMOS Inverter VM

### *Equation 1: Threshold Voltage for a MOS Transistor*

where Vinv is the input threshold.

## 1.3 Noise Margin

Noise margin is a parameter that allows us to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted. The noise margin decreases as the supply voltage decreases.

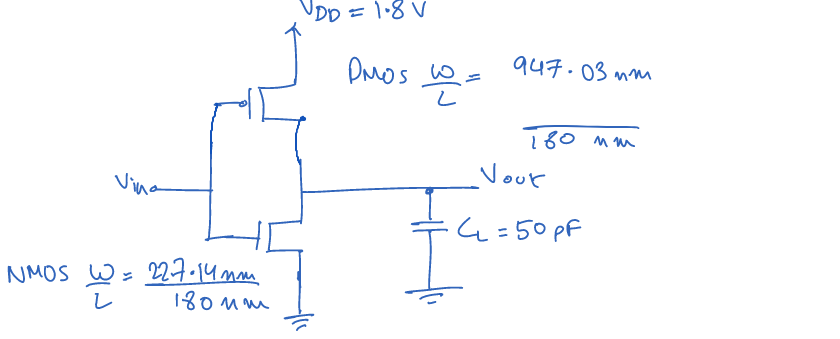
### *Equation 2: Expression for Low Noise Margin (NML) and High Noise Margin (NMH)*

## 1.4 Expression Derivation for Propagation Delay

### *Equation 3: Expression for the Propagation Delay (τp)*

## 1.5 CMOS Inverter Design

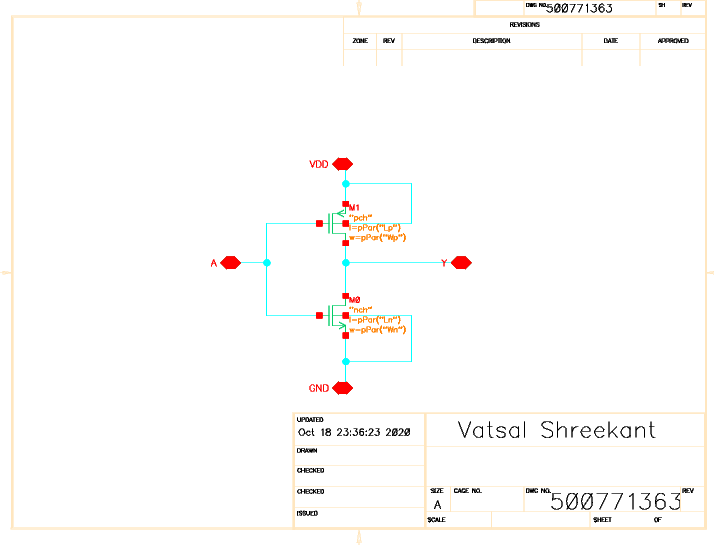
The following is the schematic for the CMOS inverter:



### *Figure 2: Schematic of CMOS Inverter*

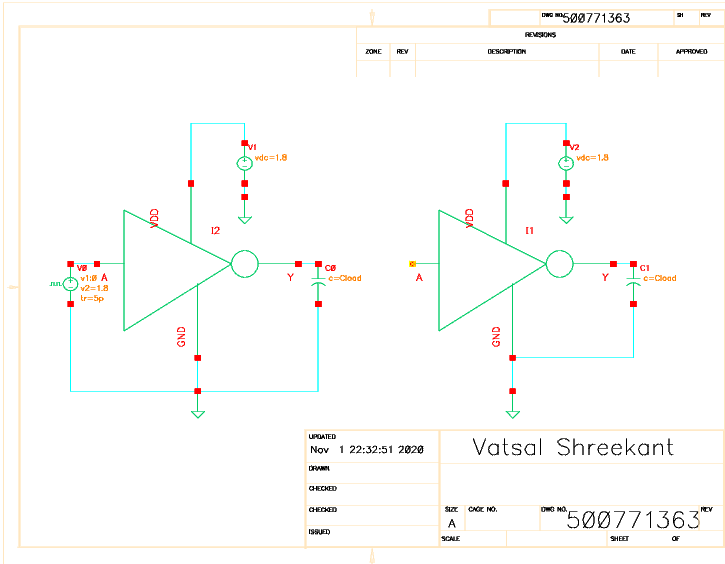
# **2. Post-Lab**

## 2.1 Schematic of CMOS Inverter



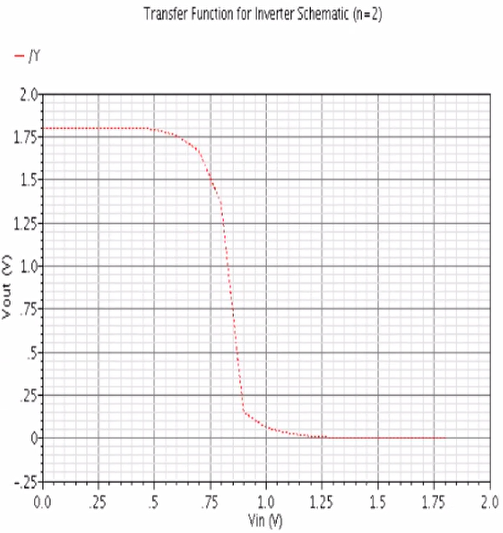
### *Figure 3: Schematic of CMOS Inverter*

## 2.2 Schematic of Testbench

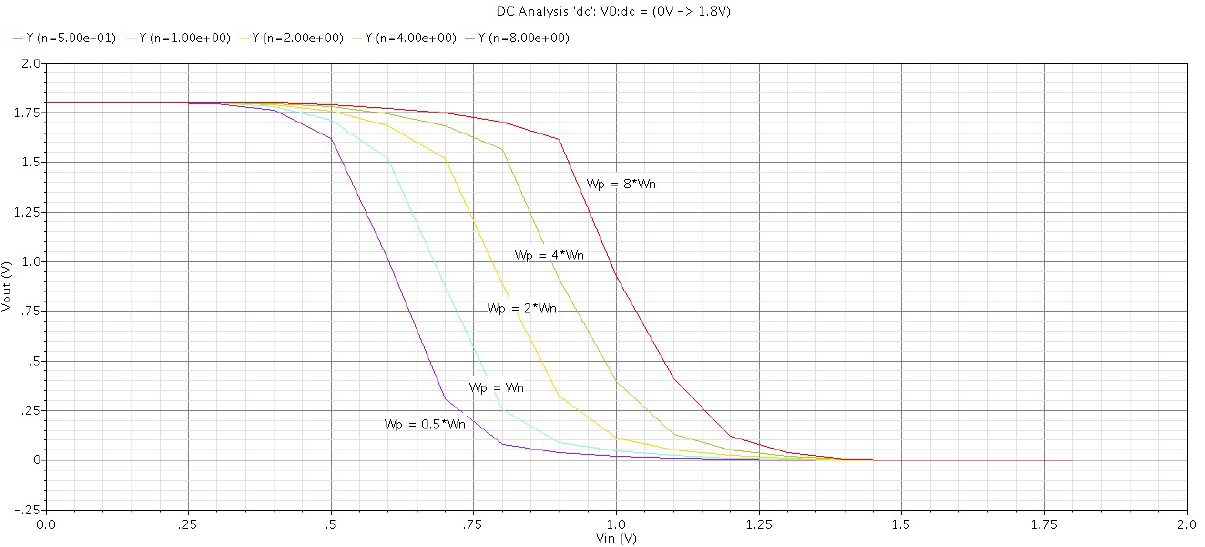


### *Figure 4: Schematic of Testbench*

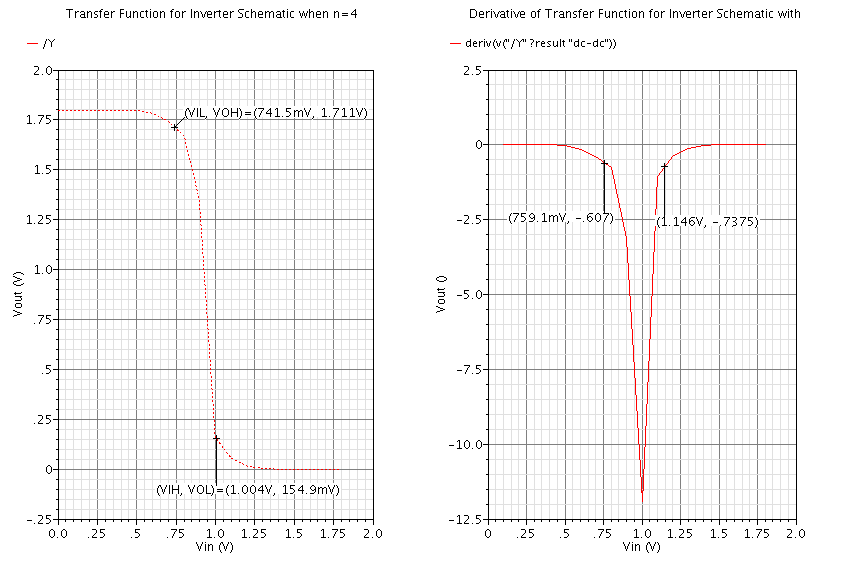
## 2.3 Results of Static and Dynamic CMOS Inverter Simulations



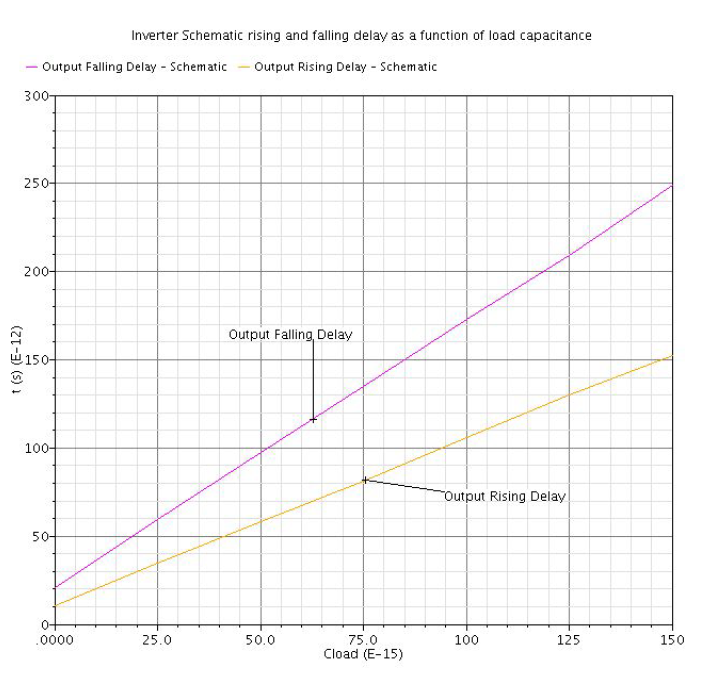
### *Figure 5:* *CMOS Inverter DC Characteristic (n=2) (Schematic)*



### *Figure 6: CMOS Inverter DC Characteristic (n=sweep) (Schematic)*



### *Figure 7: Derivative of CMOS Inverter DC Characteristic to determine VIL and VOH (Schematic)*

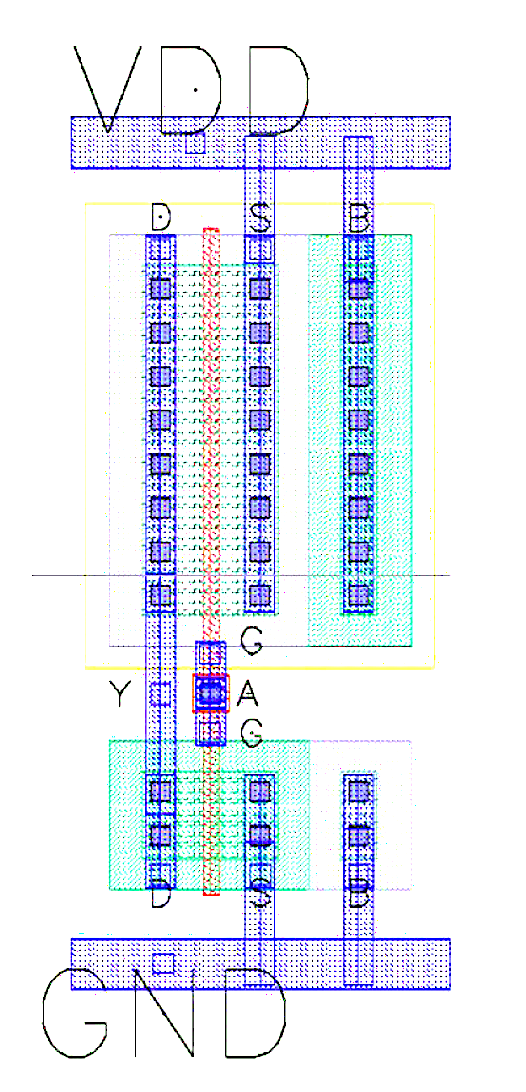


### *Figure 8: CMOS Inverter Rising and Falling Delay as Function of Load Capacitance (Schematic)*

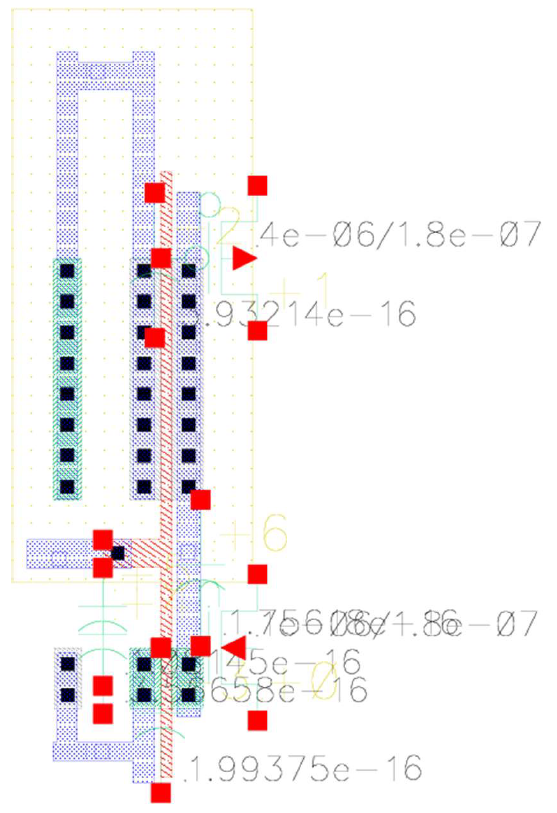
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| **Output Delay Measurements** | |
| Rising Delay (s) | 59.25p |
| Falling Delay (s) | 97.49p |

### *Table 2: Output Y Delay Measurement (Schematic)*

## 2.4 Layout and Extracted Views of CMOS Inverter

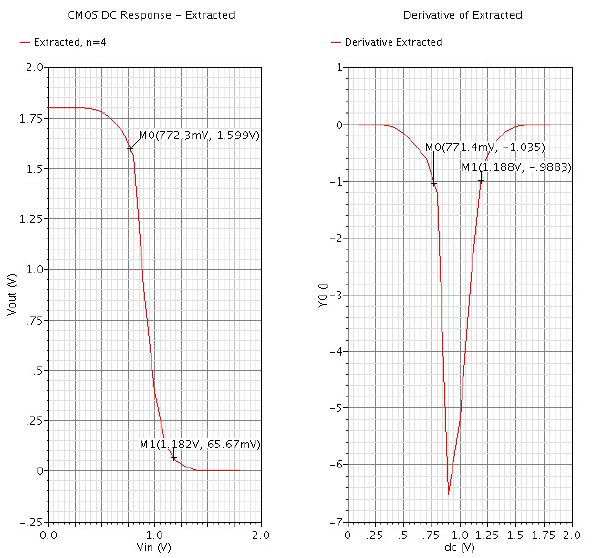


### *Figure 9: Layout View of CMOS Inverter*

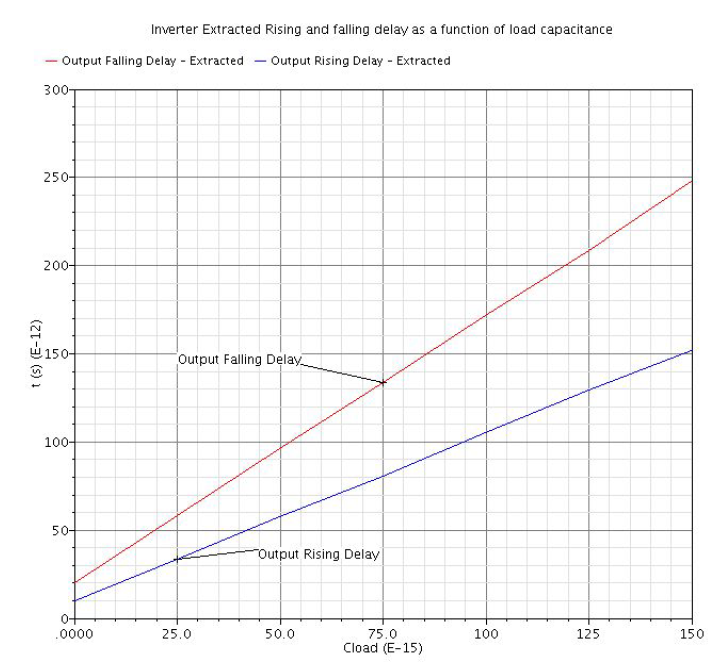


### *Figure 10: Extracted View of CMOS Inverter*

## 2.5 Post Layout Simulation Results



### *Figure 11: Derivative of CMOS Inverter DC Characteristic to Determine VIL and VOH (Extracted)*



### *Figure 12: CMOS Inverter Rising and Falling Delay as Function of Load Capacitance (Extracted)*

|  |  |
| --- | --- |
| **Output Delay Measurements** | |
| Rising Delay (s) | 58.16p |
| Falling Delay (s) | 97.20p |

### *Table 3: Output Y Delay Measurement (Extracted)*

## 3 Conclusion

This lab explored different types of characteristics and the layout of a CMOS inverter. The static and dynamic simulations were performed through Transient, DC, and Parametric analysis. From these analyses, a family of curves were created to find an ideal value for n. The ideal value for n was found to be 4 and this value was used for all the simulations. The static analysis was used on this ideal value to create its DC response and find the VIL, VOH, VIH, and VOL by calculating the derivative of the graph. The dynamic simulation was performed using transient analysis for a capacitance from 0f to 150f. The physical view for the CMOS inverter was created and used to create the extracted view. The extracted view had the same analyses applied from before with and had its static compared to the same CMOS schematic. Sizing the PMOS twice as wide as the NMOS did not lead to VM = VDD/2. Increasing the PMOS size relative to NMOS will both increase VM and reduce the rise delay.